MEMORY CONTROLLER WHICH INCREASES BUS BANDWIDTH, DATA TRANSMISSION METHOD USING THE SAME, AND COMPUTER SYSTEM HAVING THE SAME

ABSTRACT OF DISCLOSURE

A memory controller increases the effective bus bandwidth of a computer system. The memory controller includes a first port and a second port which receive and transmit N-bit data values, respectively; a third port receiving and transmitting 2N-bit data values; and a fourth port and a fifth port receiving and transmitting the N-bit data values, respectively. Here, two N-bit data values are simultaneously fetched from a memory device corresponding to the first port via the first port and a memory device corresponding to the second port in response to a command signal and an address input via the third port, the two fetched N-bit data values are combined into a 2N-bit data value, and the 2N-bit data value is transmitted to the third port. In addition, an N-bit data value is fetched from a corresponding memory device via the first port and/or second port in response to a command signal and address input via the fourth port and/or fifth port, and the fetched N-bit data value is transmitted to the fourth port and/or fifth port.

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